

# DATA SHEET

**74ABT541**

Octal buffer/line driver (3-State)

Product specification  
Supersedes data of 1996 Sep 10  
IC23 Data Handbook

1998 Jan 16

# Octal buffer/line driver (3-State)

# 74ABT541

## FEATURES

- Octal bus interface
- Functions similar to the 'ABT241
- Provides ideal interface and increases fan-out of MOS Microprocessors
- Efficient pinout to facilitate PC board layout
- 3-State buffer outputs sink 64mA and source 32mA
- Power-up 3-State
- Latch-up protection exceeds 500mA per Jedec JC40.2 Std 17

- ESD protection exceeds 2000 V per MIL STD 883 Method 3015 and 200 V per Machine Model
- Live insertion/extraction permitted

## DESCRIPTION

The 74ABT541 high-performance BiCMOS device combines low static and dynamic power dissipation with high speed and high output drive.

The 74ABT541 device is an octal buffer that is ideal for driving bus lines. The outputs are all capable of sinking 64mA and sourcing 32mA. The device features input and outputs on opposite sides of the package to facilitate printed circuit board layout.

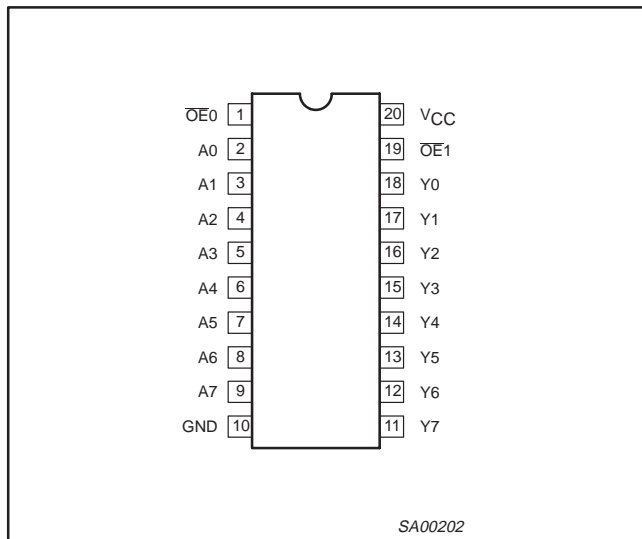
## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}\text{C}; \text{GND} = 0\text{V}$	TYPICAL	UNIT
$t_{PLH}$ $t_{PHL}$	Propagation delay An to Yn	$C_L = 50\text{pF}; V_{CC} = 5\text{V}$	2.9	ns
$C_{IN}$	Input capacitance	$V_I = 0\text{V or } V_{CC}$	4	pF
$C_{OUT}$	Output capacitance	Outputs disabled; $V_O = 0\text{V or } V_{CC}$	7	pF
$I_{CCZ}$	Total supply current	Outputs disabled; $V_{CC} = 5.5\text{V}$	500	nA

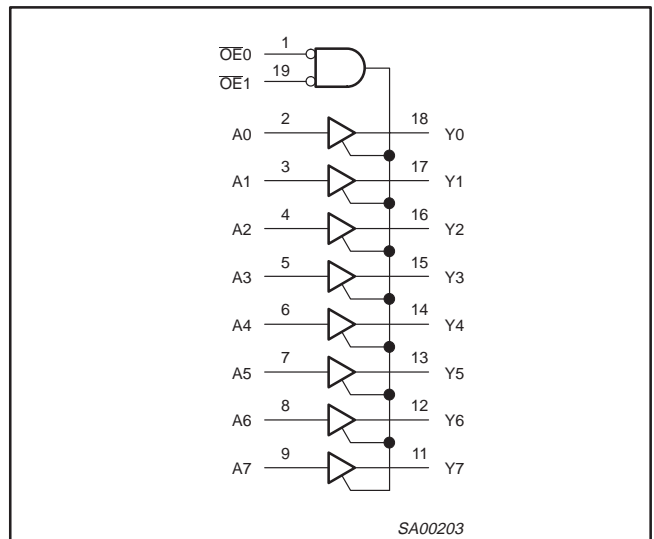
## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
20-Pin Plastic DIP	-40°C to +85°C	74ABT541 N	74ABT541 N	SOT146-1
20-Pin plastic SO	-40°C to +85°C	74ABT541 D	74ABT541 D	SOT163-1
20-Pin Plastic SSOP Type II	-40°C to +85°C	74ABT541 DB	74ABT541 DB	SOT339-1
20-Pin Plastic TSSOP Type I	-40°C to +85°C	74ABT541 PW	74ABT541PW DH	SOT360-1

## PIN CONFIGURATION



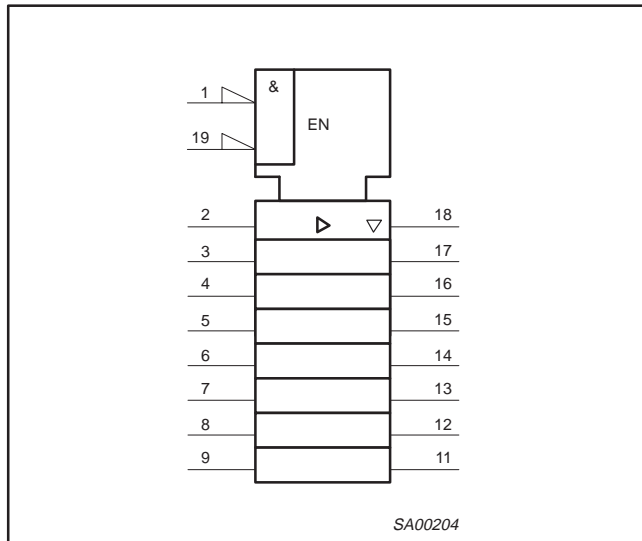
## LOGIC SYMBOL



# Octal buffer/line driver (3-State)

# 74ABT541

## LOGIC SYMBOL (IEEE/IEC)



## PIN DESCRIPTION

PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 3, 4, 5, 6, 7, 8, 9	A0 – A7	Data inputs
18, 17, 16, 15, 14, 13, 12, 11	Y0 – Y7	Data outputs
1, 19	$\overline{OE}0, \overline{OE}1$	Output enables
10	GND	Ground (0V)
20	V <sub>CC</sub>	Positive supply voltage

## FUNCTION TABLE

INPUTS			OUTPUTS
$\overline{OE}0$	$\overline{OE}1$	A <sub>n</sub>	Y <sub>n</sub>
L	L	L	L
L	L	H	H
X	H	X	Z
H	X	X	Z

H = High voltage level  
 L = Low voltage level  
 X = Don't care  
 Z = High impedance "off" state

## ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V <sub>CC</sub>	DC supply voltage		-0.5 to +7.0	V
I <sub>IK</sub>	DC input diode current	V <sub>I</sub> < 0	-18	mA
V <sub>I</sub>	DC input voltage <sup>3</sup>		-1.2 to +7.0	V
I <sub>OK</sub>	DC output diode current	V <sub>O</sub> < 0	-50	mA
V <sub>OUT</sub>	DC output voltage <sup>3</sup>	output in Off or High state	-0.5 to +5.5	V
I <sub>OUT</sub>	DC output current	output in Low state	128	mA
T <sub>stg</sub>	Storage temperature range		-65 to 150	°C

### NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		Min	Max	
V <sub>CC</sub>	DC supply voltage	4.5	5.5	V
V <sub>I</sub>	Input voltage	0	V <sub>CC</sub>	V
V <sub>IH</sub>	High-level input voltage	2.0		V
V <sub>IL</sub>	Low-level Input voltage		0.8	V
I <sub>OH</sub>	High-level output current		-32	mA
I <sub>OL</sub>	Low-level output current		64	mA
Δt/Δv	Input transition rise or fall rate	0	5	ns/V
T <sub>amb</sub>	Operating free-air temperature range	-40	+85	°C

## DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS					UNIT
			T <sub>amb</sub> = +25°C			T <sub>amb</sub> = -40°C to +85°C		
			Min	Typ	Max	Min	Max	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = 4.5V; I <sub>IK</sub> = -18mA		-0.9	-1.2		-1.2	V
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = 4.5V; I <sub>OH</sub> = -3mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	2.5	2.9		2.5		V
		V <sub>CC</sub> = 5.0V; I <sub>OH</sub> = -3mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	3.0	3.4		3.0		V
		V <sub>CC</sub> = 4.5V; I <sub>OH</sub> = -32mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>	2.0	2.4		2.0		V
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = 4.5V; I <sub>OL</sub> = 64mA; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>		0.42	0.55		0.55	V
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 5.5V; V <sub>I</sub> = GND or 5.5V		±0.01	±1.0		±1.0	μA
I <sub>OFF</sub>	Power-off leakage current	V <sub>CC</sub> = 0.0V; V <sub>I</sub> or V <sub>O</sub> ≤ 4.5V		±5.0	±100		±100	μA
I <sub>PU</sub> /I <sub>PD</sub>	Power-up/down 3-state output current <sup>3</sup>	V <sub>CC</sub> = 2.0V; V <sub>O</sub> = 0.5V; V <sub>I</sub> = GND or V <sub>CC</sub> ; V <sub>OE</sub> = Don't care		±5.0	±50		±50	μA
I <sub>OZH</sub>	3-State output High current	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 2.7V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>		5.0	50		50	μA
I <sub>OZL</sub>	3-State output Low current	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 0.5V; V <sub>I</sub> = V <sub>IL</sub> or V <sub>IH</sub>		-5.0	-50		-50	μA
I <sub>CEx</sub>	Output High leakage current	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 5.5V; V <sub>I</sub> = GND or V <sub>CC</sub>		5.0	50		50	μA
I <sub>O</sub>	Output current <sup>1</sup>	V <sub>CC</sub> = 5.5V; V <sub>O</sub> = 2.5V	-40	-100	-180	-40	-180	mA
I <sub>CCH</sub>	Quiescent supply current	V <sub>CC</sub> = 5.5V; Outputs High, V <sub>I</sub> = GND or V <sub>CC</sub>		0.5	250		250	μA
I <sub>CCL</sub>		V <sub>CC</sub> = 5.5V; Outputs Low, V <sub>I</sub> = GND or V <sub>CC</sub>		24	30		30	mA
I <sub>CCZ</sub>		V <sub>CC</sub> = 5.5V; Outputs 3-State; V <sub>I</sub> = GND or V <sub>CC</sub>		0.5	250		250	μA
ΔI <sub>CC</sub>	Additional supply current per input pin <sup>2</sup>	Outputs enabled, one input at 3.4V, other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5V		0.5	1.5		1.5	mA
		Outputs 3-State, one data input at 3.4V, other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5V		0.5	50		50	μA
		Outputs 3-State, one enable input at 3.4V, other inputs at V <sub>CC</sub> or GND; V <sub>CC</sub> = 5.5V		0.5	1.5		1.5	mA

## NOTES:

- Not more than one output should be tested at a time, and the duration of the test should not exceed one second.
- This is the increase in supply current for each input at 3.4V.
- This parameter is valid for any V<sub>CC</sub> between 0V and 2.1V with a transition time of up to 10msec. For V<sub>CC</sub> = 2.1V to V<sub>CC</sub> = 5V ± 10%, a transition time of up to 100μsec is permitted.

# Octal buffer/line driver (3-State)

# 74ABT541

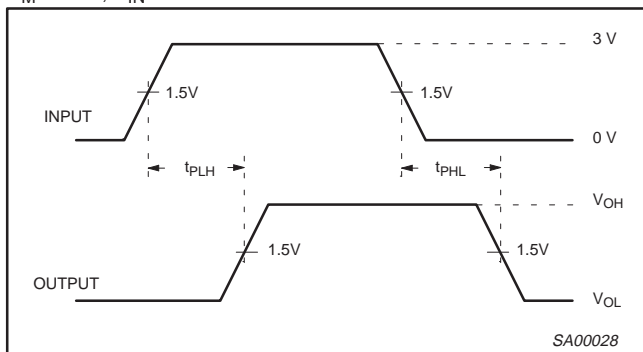
## AC CHARACTERISTICS

GND = 0V;  $t_R = t_F = 2.5\text{ns}$ ;  $C_L = 50\text{pF}$ ,  $R_L = 500\Omega$

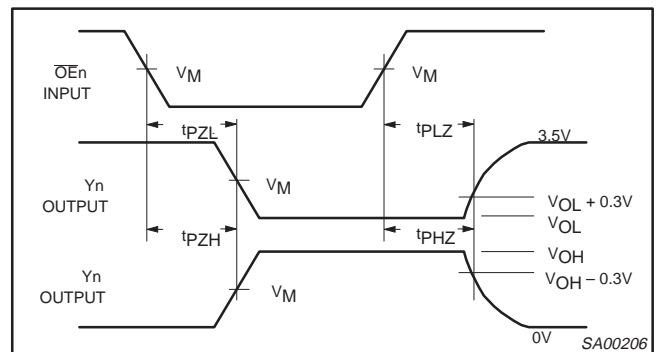
SYMBOL	PARAMETER	WAVEFORM	LIMITS					UNIT
			$T_{\text{amb}} = +25^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V}$			$T_{\text{amb}} = -40^\circ\text{C to } +85^\circ\text{C}$ $V_{\text{CC}} = +5.0\text{V} \pm 0.5\text{V}$		
			Min	Typ	Max	Min	Max	
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation delay An to Yn	1	1.0	2.6	4.1	1.0	4.6	ns
$t_{\text{PZH}}$ $t_{\text{PZL}}$	Output enable time to High and Low level	2	1.1	3.1	4.8	1.1	5.3	ns
$t_{\text{PHZ}}$ $t_{\text{PLZ}}$	Output disable time from High and Low level	2	2.1	5.1	6.6	2.1	7.1	ns

## AC WAVEFORMS

$V_M = 1.5\text{V}$ ,  $V_{\text{IN}} = \text{GND to } 3.0\text{V}$



Waveform 1. Waveforms Showing the Input (An) to Output (Yn) Propagation Delays



Waveform 2. Waveforms Showing the 3-State Output Enable and Disable Times

## TEST CIRCUIT AND WAVEFORMS

TEST	S1
$t_{\text{pd}}$	open
$t_{\text{PLZ}}/t_{\text{PZL}}$	7 V
$t_{\text{PHZ}}/t_{\text{PZH}}$	open

**DEFINITIONS**  
 $C_L =$  Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

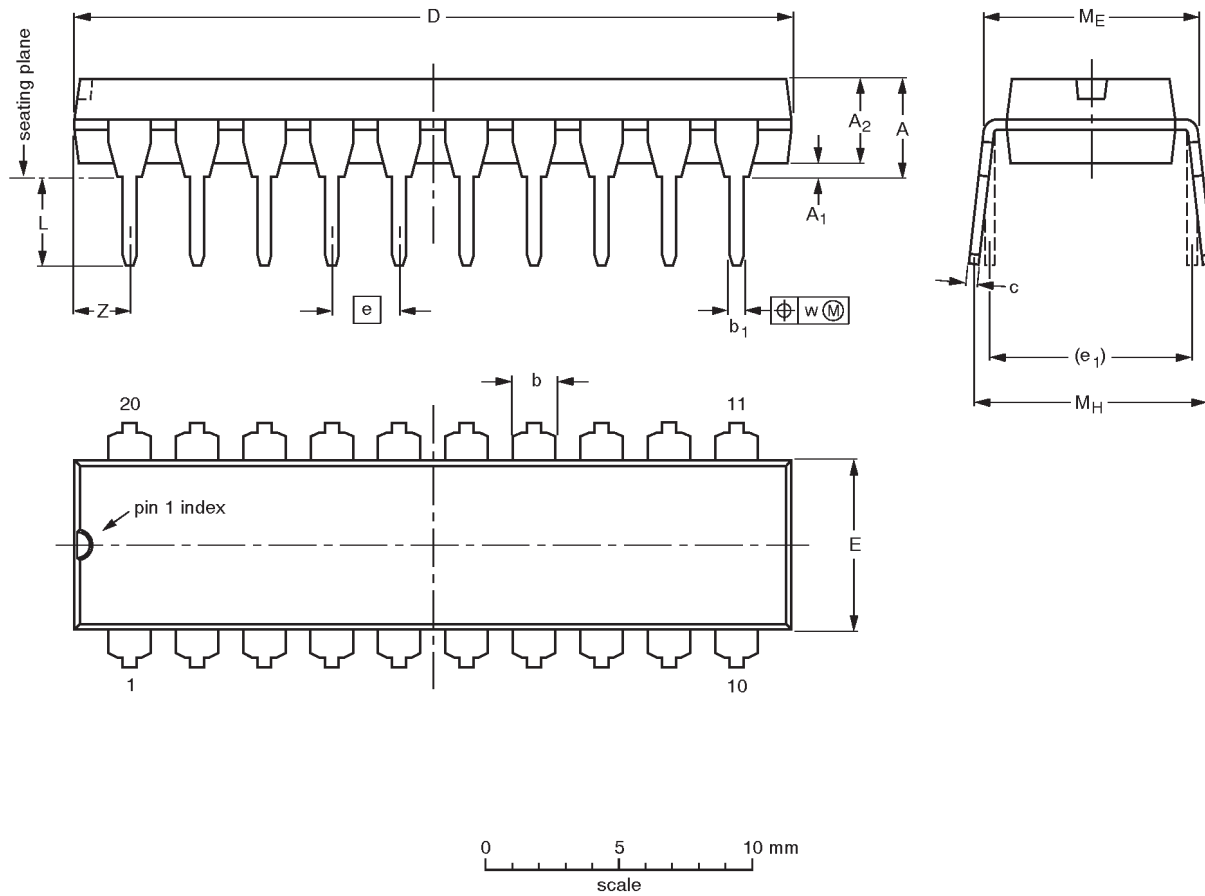
SA00012

# Octal buffer/line driver (3-State)

# 74ABT541

**DIP20: plastic dual in-line package; 20 leads (300 mil)**

**SOT146-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub> min.	A <sub>2</sub> max.	b	b <sub>1</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	e <sub>1</sub>	L	M <sub>E</sub>	M <sub>H</sub>	w	Z <sup>(1)</sup> max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	0.36 0.23	26.92 26.54	6.40 6.22	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	2.0
inches	0.17	0.020	0.13	0.068 0.051	0.021 0.015	0.014 0.009	1.060 1.045	0.25 0.24	0.10	0.30	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.078

**Note**

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT146-1			SC603			92-11-17 95-05-24

# Octal buffer/line driver (3-State)

# 74ABT541

**SO20:** plastic small outline package; 20 leads; body width 7.5 mm

**SOT163-1**



**DIMENSIONS (inch dimensions are derived from the original mm dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				92-11-17 95-01-24

# Octal buffer/line driver (3-State)

# 74ABT541

**SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm**

**SOT339-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

**Note**

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				93-09-08 95-02-04



# Octal buffer/line driver (3-State)

## 74ABT541

**TSSOP20:** plastic thin shrink small outline package; 20 leads; body width 4.4 mm

**SOT360-1**



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				-93-06-16 95-02-04

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Octal buffer/line driver (3-State)

74ABT541

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**NOTES**

## Octal buffer/line driver (3-State)

74ABT541

## Data sheet status

Data sheet status	Product status	Definition [1]
Objective specification	Development	This data sheet contains the design target or goal specifications for product development. Specification may change in any manner without notice.
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[1] Please consult the most recently issued datasheet before initiating or completing a design.

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print code

Date of release: 05-96

Document order number:

9397-750-03614

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